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Title:

METAL CARBIDE GATE STRUCTURE AND METHOD OF FABRICATION

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METAL CARBIDE GATE STRUCTURE AND METHOD OF FABRICATION

TECHNICAL FIELD

The present invention relates to gate structures comprising metal carbides. This invention finds special applicability in complementary metal oxide semiconductor (CMOS) devices incorporating dual work function metal gate electrodes. More particularly, the present invention relates to dual work function metal gates wherein the dual work functions are provided by a metal and a carbide of a metal.

The present invention also relates to methods for fabricating the metal gate devices of the present invention.

BACKGROUND OF THE INVENTION

Advanced complementary metal oxide semiconductor (CMOS) devices are increasingly utilizing metal gate electrodes in order to avoid the "poly-Si depletion" and "boron penetration" effects observed with traditional gate electrodes of doped polycrystalline silicon (poly-Si). The selection of a particular metal for a gate material is guided by a number of considerations, including the work function and electrical resistivity desired for the gate, the thermal budget that the gate metal will be expected to survive, the type of gate dielectric (high-k or conventional), and the existence of a damage-free gate metal deposition process. Though mid-gap metals such as tungsten might be usable for both n-type field effect transistors (n-FETs) and p-type FETs (p-FETs) in CMOS, it is desirable to use one (high work function) gate metal appropriate for p-FETs and another (low work function) gate metal appropriate for n-FETs, in a design approach known as "dual metal/dual work function" CMOS.

Such dual metal/dual work function schemes can be very complex if the two different metals require different deposition and patterning processes. This is especially true when the patterning is done subtractively, since the second metal to be deposited must be removed without damaging the first. The complexity of such dual metal/dual work function schemes for CMOS metal gates has thus led to increased interest in "single metal/dual work function" schemes in

which a single gate material is deposited over n-FET and p-FET device areas and then modified so that it has an n-FET-appropriate work function in n-FET device areas and a p-FET-appropriate work function in p-FET device areas.

Approaches to "single metal/dual work function" have been described in the literature. One approach [V. Misra et al., IEEE Electron Device Letters 23 354 (2002) and H. Zhong et al., IEDM Tech. Dig. 467 (2001)], suggests depositing a Ru-Ta alloy layer with an n-FET work function over n-FET and p-FET device areas and then converting the Ru-Ta alloy into a Ru-rich Ru-Ta alloy with a p-FET work function (in the p-FET device areas) by depositing additional Ru and annealing.

In another approach, a metal such as Mo with a p-FET work function is deposited over n-FET and p-FET device areas and converted into a Mo nitride having a n-FET work function (in n-FET device regions) by either ion implantation of nitrogen [P. Ranade et al., Mat. Res. Soc. Proc. 670 K5.2 (2001); R. Lin et al., IEEE Electron Device Letters 23 49 (2002)] or solid state diffusion/reaction of nitrogen from an N-rich overlayer of TiN [R.J.P. Lander et al., Mat. Res. Soc. Symp. Proc. 716 B5.11 (2002)].

A drawback of the nitrogen ion implantation approach is that it can damage the underlying gate dielectric [T. Amada et al., Mat. Res. Soc. Symp. Proc. 716 B7.5 (2002)]. Solid state diffusion of nitrogen from TiN results in less damage, but does not quite provide sufficient change in the work function ($\sim$ -0.5 eV observed for Mo on SiO_2, $\sim$-0.75 eV is desired). Drawbacks of the Ru-Ta alloy approach include the potential for tantalum reaction with the gate dielectric, and the lack of chemical vapor deposition (CVD) methods for the Ru-Ta alloy (since CVD is one of the few deposition processes that is free from dielectric-damaging charged particle bombardment).

SUMMARY OF INVENTION

The present invention relates to providing alternative methods for forming single metal/dual work function gate electrodes for CMOS. The present invention addresses problems described above.

The present invention relates to a semiconductor device containing source drain/regions and gate regions wherein at least one gate electrode comprises a metal carbide obtained by reacting a metal and a carbon-containing layer .

A further aspect of the present invention relates to a dual work function complementary metal oxide semiconductor (CMOS) circuit which comprises at least one FET having a gate electrode formed from a conductive material, and at least one FET having a gate electrode comprising a metal carbide obtained by reacting a metal and a carbon-containing layer, wherein the metal differs from the conductive material.

This invention additionally relates to a dual work function complementary metal oxide semiconductor (CMOS) circuit which comprises
-at least one FET having a gate electrode formed from a first metal, and
-at least one FET having a gate electrode formed from a carbide of said first metal.

Another aspect of the present invention relates to a method of forming a gate for a FET which comprises providing a substrate, and depositing on said substrate a metal and a carbon-containing layer and reacting said metal and carbon-containing layer to form a metal carbide for providing a gate electrode.

A still further aspect of the present invention is concerned with a method of forming a dual work function CMOS device on a substrate. The method comprises:
depositing a metal layer on a first and second set of gate regions;
providing a carbon-containing layer in contact with one of said first and second set of gate regions and not on the other of said first and second set of gate regions, said carbon-containing layer being in direct contact with said metal layer on said one of said first and second set of gate regions;
reacting said carbon-containing layer on said one of said first and second set of gate regions with said metal on said one of said first and second set of gate regions to form a metal carbide.
Other objectives and advantages of the present invention will become readily apparent to those skilled in this art from the following detailed description, wherein it is shown and

described only the preferred embodiments of the invention simply by way of illustration of the best mode contemplated of carrying out the invention. As will be realized, the invention is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects, without departing from the invention. Accordingly, the description is to be regarded as illustrative in nature and not as restrictive.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A – 1E show, in cross-section view, the basic steps of a method of the present invention for fabricating CMOS gate electrodes;

Figs. 2A - 2D show a first variation of the method of Fig. 1;

Figs. 3A - 3D show a second variation of the method of Fig. 1;

Figs. 4A - 4D show a third variation of the method of Fig. 1;

Figs. 5A - 5H show a variation of the method of Fig. 1 adapted for a replacement gate process flow;

Figs. 6A – 6C compare Mo carbide formation for sample geometries corresponding to three embodiments of the invention; and

Fig. 7 shows capacitance-voltage (C-V) measurements used to determine the work functions of mo and Mo_2C capacitor electrodes.

DESCRIPTION OF BEST AND VARIOUS EMBODIMENTS

The present invention relates to semiconductor structures comprising at least one FET having a gate electrode. In order to facilitate an understanding of the present invention, the detailed description relates to the preferred aspect of "single metal dual work function" metal gates.

According to preferred aspects, the present invention provides a new approach to "single metal/dual work function" metal gates wherein the dual work functions are provided by a metal and a carbide of the metal.

Accordingly, one aspect of the present invention relates to a dual work function complementary metal oxide semiconductor (CMOS) circuit which comprises
-at least one FET having a gate electrode formed from a first metal, and
-at least one FET having a gate electrode formed from a carbide of said first metal.

The present invention also provides a dual work function CMOS circuit which comprises
-at least one FET having a gate electrode formed from a first metal and at least one additional element and
-at least one FET having a gate electrode formed from a carbide of said first metal.

The dual work function CMOS structures according to the present invention can be fabricated by depositing a metal with a first work function over both n-FET and p-FET device areas, and then reacting with a carbon-containing layer in selected areas to form a metal carbide with a second work function different from the first work function. For the purposes of the present invention, the term "carbide" is defined as a compound or mixture of carbon with one or more elements more electropositive than carbon.

One process technique for fabricating the dual work function CMOS structures on a substrate according to the present invention comprises:

- depositing a metal layer with a first work function;
- patterning the metal layer to form a first and second set of gate-shaped structures;

- forming a patterned a layer of carbon-containing material so that the carbon-containing material is disposed on one of the first and second set of gate-on the substrate shaped structures and absent from other of the first and second set of gate shaped structures

- reacting the patterned carbon-containing material with the metal in regions where both are present to form a material with a second work function;

- optionally removing carbon residuals remaining after the reaction; and

- optionally annealing in an inert or reactive ambient to repair any processing damage.

Examples of providing the patterned carbon-containing layer include

depositing a carbon-containing layer and patterning said carbon-containing layer by selectively removing it from one of said first and second set of gate regions by a process such as reactive ion etching while leaving it remaining on the other of said first and second set of gate regions; and

depositing and patterning a photoresist layer, blanket-depositing a carbon-containing layer on said photoresist layer and then removing said photoresist along with the carbon-containing layer located on top of the photoresist while leaving the carbon-containing layer not located on top of the photoresist.

Reference to Figures 1A-1E illustrates the above sequence for fabricating dual work function CMOS structures according to the present invention.

Fig. 1A shows substrate 10 after deposition of metal layer 20 having a first work function. Substrate 10 typically begins as one or more semiconductor layers under an insulating gate dielectric and eventually comprises dielectric isolation regions, heavily doped semiconductor source/drain regions, and lightly doped or undoped semiconductor channel regions. Fig. 1B shows the structure of Fig. 1A after metal layer 20 has been patterned to form metal gate structures 30. Fig. 1C shows the structure after formation of a patterned of carbon-containing layer 40. The structure of Fig. 1C is annealed to produce metal carbide gate structure 50 having a second work function, and leftover carbon-containing layer 60. Leftover carbon-containing layer 60 may then be removed by a process such as an oxygen plasma treatment to produce the structure of Fig. 1E with metal gate 30 with a first work function and metal carbide gate 50 with a second work function.

In the process flow shown in Fig. 1A-1E, metal layer 20 is deposited and patterned to form metal gate structures before deposition of patterned carbon-containing layer 40. However, the steps of the process may be implemented in a variety of permutations. For example, gate patterning may be done before or after carbon deposition; carbon deposition may be done before or after metal deposition; and carbide formation may be done before or after gate patterning.

Figs. 2 and 3 show two examples of process flows in which gate electrode patterning is done after the metal and patterned carbon-containing layers are deposited. In the process flow of Figs. 2A - 2D, carbide formation takes place after gate patterning. Fig. 2A shows substrate 10 after deposition of metal layer 20 having a first work function. Fig. 2B shows the structure of Fig. 2A after deposition of patterned carbon-containing layer 40. Fig. 2C shows the structure after gate patterning to form metal gates 30 and gate-shaped carbon-containing layer 70. The structure of Fig. 2C is then annealed to produce the structure of Fig. 2D with metal gate 30 with a first work function and metal carbide gate 50 with a second work function. Remnants of gate-shaped carbon-containing layer 70 remaining after the anneal may be removed by a process such as an oxygen plasma treatment.

In the process flow of Figs. 3A - 3D, carbide formation takes place before patterning. Fig. 3A shows substrate 10 after deposition of metal layer 20 having a first work function. Fig. 3B shows the structure of Fig. 3A after deposition of patterned carbon-containing layer 40. The structure of Fig. 3B is then annealed to produce the structure of Fig. 3C with metal carbide layer 80. Metal layer 20 and metal carbide layer 80 are then patterned to form metal gate 30 with a first work function and metal carbide gate 50 with a second work function. Remnants of gate-shaped carbon-containing layer 40 remaining after the anneal may be removed by a process such as an oxygen plasma treatment.

The process can also be implemented with the carbon-containing layer deposited before the metal layer. This is shown in Fig. 4 for a process flow in which the carbide formation anneal is performed before gate patterning, in a process flow analogous to that of Fig. 3. Fig 4A shows substrate 10 after deposition of patterned carbon-containing layer 40. Fig. 4B shows the structure after deposition of metal layer 90 having a first work function. The structure of 4B is then annealed to produce the structure of Fig. 4C with metal carbide layer 80. Metal layer 90 and

metal carbide layer 80 are then patterned to form metal gate 30 with a first work function and metal carbide gate 50 with a second work function. Remnants of metal layer 90 remaining above metal carbide layer 80 would typically be left in place, since the additional metal would not be expected to affect the work function at the metal carbide/substrate interface.

Figs. 5A - 5H show how the invention could be implemented for the case of a replacement gate process flow [see, for example, B. Guillaumot et al., IEDM Tech. Digest, p. 355 (2002)]. Fig. 5A shows substrate 120 with a first gate cavity region 130 and second gate cavity region 140; Fig. 5B shows the structure of Fig. 5A after deposition of a blanket-deposited metal layer 150 having a first work function, and Fig. 5C shows the structure of after blanket deposition of carbon-containing layer 160. Fig. 5D shows the structure of Fig. 5C after carbon-containing layer 160 has been patterned to form patterned carbon-containing layer 165 which is disposed on gate cavity region 140 and absent from gate cavity region 130. The structure of Fig. 5D is then annealed to produce metal carbide 180 and leftover carbon-containing layer 185 (Fig. 5E) in gate cavity region 140. Leftover carbon-containing layer 185 is then removed by an oxygen plasma treatment to produce the structure of Fig. 5F with metal gate 150 having a first work function and metal carbide gate 180 having a second work function. The structure of Fig. 5F would ordinarily be completed by filling gate cavity regions 130 and 140 with a conductive material 190 (Fig. 5G), and then planarizing to form completed metal first gate 200 and completed metal carbide second gate 210 (Fig. 5H).

In cases where the metal and the metal's carbide do not provide sufficiently different work functions, it may be desirable to extend the methods of this invention to modify the work function of the metal that is not carbided. Modifications to the metal that is not carbided may be performed (i) before or after carbide formation, and (ii) before or after gate patterning. The modifications may be effected by processes such as alloying, mixing, or reaction with at least one additional element, implantation with one or more species of ions, etc. For example, single metal dual work function CMOS gates may be fabricated from a mid-gap metal by carbiding the mid-gap metal to form a first set of gates with a first work function, and alloying or implanting the non-carbided mid-gap metal with one or more elements to form a second set of gates with a second work function.

Metals that may be considered for the metal/metal carbide processes of the present invention include any conductive materials, for example, Al, Ba, Be, Bi, Co, Cr, Cu, Dy, Fe, Ga, Gd, Ir, Hf, Mg, Mo, Mn, Nb, Ni, Pd, Pt, Ir, La, Os, Pr, Nb, Rh, Re, Ru, Sc, Sn, Ta, Ti, V, W, Y, Zn, and Zr; conductive nitrides, silicides, germanides, and silicon nitrides of these metals or their alloys; conductive alloys or compounds of these metals with or without additional nonmetallic elements.

Deposition techniques for these metals may include thermal evaporation, electron-beam evaporation, sputtering, reactive sputtering, ion beam sputtering, electroless deposition, CVD, metal-organic CVD (MOCVD), plasma-enhanced CVD (PECVD), and atomic layer deposition (ALD).

Preferred metals for this process include Mo, Mo-Ru alloys, and other p-FET (high work function) metals that form carbides. Preferred metal deposition techniques for this process include CVD and MOCVD because there is no energetic charged particle bombardment tending to damage the gate dielectric.

The carbon-containing layers of this process may include any carbon-containing material deposited by any method. The carbon-containing layers may comprise, for example, diamond, graphite; amorphous carbon with minimal H content; amorphous hydrogenated carbon (a-C:H, also known as diamond-like-carbon or DLC); carbon-containing polymers such as poly(methyl)methacrylate, polyimide, SiLK; organic photoresists; amorphous carbon-containing layers containing other elements such as Si, O, N, and/or H (e.g., SiCOH or SiCH).

Deposition methods for these carbon-containing layers may include spin-on techniques, solution-casting techniques, CVD, plasma-assisted CVD (PACVD), plasma-enhanced CVD (PECVD), thermal evaporation, electron-beam evaporation, sputter deposition from a carbon-containing target using an inert or reactive working gas, ion beam sputtering. It should be noted that certain carbon-containing layers may require stabilization anneals if they are deposited before the metal. For example, a carbon-containing layer of DLC is typically given a stabilization anneal (e.g., 400 °C for 4 hrs in He) prior to metal deposition to prevent blistering during carbide formation.

Preferred carbon-containing layers include pure carbon deposited by physical sputtering and amorphous hydrogenated carbon (also known as diamond-like carbon or DLC) deposited by PECVD.

The carbon layer is easily patterned (by oxygen-based reactive ion etching, for example) so that it remains only over n-FET device areas. When metal carbide formation is complete, the excess carbon remaining may be selectively removed by an oxygen-based ashing or reactive ion etching plasma. The metal Mo and its carbides are both quite resistant to oxidation.

If desired, the electrode stacks may be annealed in an inert or reactive ambients to repair any process damage and/or to improve the device characteristics. This annealing may be performed at any stage of the process.

The metal layers of this invention typically have a thickness of about 2 to about 500 nanometers, more typically about 5 to about 50 nanometers. The optimum thickness for the carbon-containing layers of this invention will depend on several factors: the stoichiometry of the desired carbide (e.g., MC, M_2C, M_3C, where M denotes the metallic element being carbided), the thickness of the metal layer, the carbon content of the carbon-containing layer (e.g., sputtered deposited C has a higher carbon content than a-C:H), and the order of the layers (a slight excess of carbon might be desirable if the metal is under the carbon, whereas a slight excess of metal might be desirable if the carbon is under the metal). The areal density of metal atoms (atoms/cm^2) in a metal layer may be computed from the metal's thickness, density, and molecular weight (MW). A Mo layer 30 nanometers in thickness would be expected to have an areal density of 1.9e17 Mo atoms/cm^2 (based on a MW of 96 g/mole and a density of 10.2 g/cm^3). The thickness of an amorphous carbon layer needed to provide exactly half this number of C atoms (to make Mo_2C) would be 9.5 nanometers (given a MW of 12 g/mole and a density of 2 g/cm^3).

The annealing temperature/time conditions typical for carbide formation depend on the identity of the metal and the stoichiometry of the desired carbide. Annealing for higher temperatures or longer times than needed to form a desired first carbide (such as M_2C) might lead to further reaction and formation of an undesired second carbide with a higher carbon

content (such as MoC). The optimum annealing will also depend, to a lesser extent, on the metal film thickness and the type of carbon (e.g., sputtered deposited C vs. a-C:H). Carbide formation in carbide-forming metals will typically occur at temperatures of about 400 to about 1100 °C. Interestingly, carbide formation at the lower end of this temperature range may be facilitated by incorporation of hydrogen [A. Rubinshtein et al., "Surface treatment of tantalum to improve its corrosion resistance, "Mater. Sci. Eng. A A302, 128 (2001)]. Annealing ambients are typically be selected from the following gases and their mixtures: Ar, He, H_2, N_2, CHx. N_2, and forming gas. N_2 would be a less preferred ambient for metals readily forming nitrides. The annealing time required for completion of the carbide reaction will depend on the temperature; for a given metal and metal thickness, the required annealing time will decrease as the annealing temperature increases.

Carbide forming metals include Cr, Fe, Hf, Mn, Mo, Nb, Ni, Ta, Ti, V, W, and others. Of these, Fe is among the metals forming carbides at the low end of the 400-1000 °C temperature range and W is among the metals forming carbides at the high end of this temperature range. Typically a rapid thermal anneal at about 750 °C for about 1 min in N_2 is sufficient to completely convert a bilayer film of C on Mo (30 nanometers) to Mo_2C.

Figs. 6A - 6C examine Mo carbide formation for sample geometries corresponding to three embodiments of the invention: a blanket Mo layer over a layer of sputtered carbon, a blanket Mo layer over a layer of DLC (annealed for 4 hours at 400 °C in He prior to metal deposition), and a blanket Mo layer under a layer of sputtered carbon. The Mo in all samples is 30 nanometers thick and deposited by sputtering. Carbide formation is monitored during rapid thermal annealing (at 3 °C/sec in a He ambient) by in situ x-ray diffraction (XRD) with synchrotron radiation having a wavelength of 0.1797 nanometers, intensity of 10^{13} photons/s and energy resolution of 1.5% [G.B. Stephenson et al., Rev. Sci. Instrum. 60 1537 (1989)].

All samples initially show a single XRD peak at $2\theta = 48o$, corresponding to the Mo 110 reflection. Carbide formation is indicated by the disappearance of the Mo 110 peak and the appearance of hexagonal Mo_2C peaks at 47o (Mo_2C 101), 45o (Mo_2C 002) and 40.5o (Mo_2C 100). The plot of Fig. 6A, for a sputtered Mo layer on top of a 200 nanometers-thick sputtered C layer, shows a sharply defined reaction around 775 °C. The plot of Fig. 6B, for a nominally

identical sputtered Mo layer on top of a 180 nanometers-thick layer of DLC, shows a slightly broader reaction that is also centered around 775 °C. The plot of Fig. 6C, for a sputtered Mo layer under a 30 nanometers-thick layer of sputtered C, shows an even broader reaction centered around a slightly lower temperature (~760 °C). The thermal treatments needed for carbide formation in these cases is thus well within typical thermal budgets for CMOS.

The electrical measurements of Fig. 7 verify that the work function of Mo is substantially lowered upon carbide formation. Capacitance-voltage (C-V) measurements were performed on Si(substrate)/SiO$_2$(5 or 11 nanometers)/Mo(C) capacitors with Mo and Mo carbide electrodes. Mo(30 nanometers) and Mo(30nanometers, bottom)/C(10nanometers, top) electrode films are sputter deposited through a Si membrane mask with electrode area openings of 6.2e-04 cm or 9.5e-05 cm onto oxide-coated n-type single crystal (100) Si. Both Mo and Mo/C electrodes receive "carbide formation" anneals (3°C/sec ramp to 900°C in forming gas) sufficient to convert the Mo/C electrode to Mo$_2$C. Fig. 7 shows data for the case of 5 nanometers SiO$_2$. Analysis of the C-V slopes and voltage intercepts indicate a work function of 4.50-4.60 eV for Mo and one of 4.25-4.35 eV for Mo$_2$C.

Moreover, as mentioned above, the metal carbides such as those formed by the solid state reaction of a first metal with a carbon-containing layer may also be used as gate electrodes in single FETs, in pluralities of FETs, and in dual work function CMOS circuits where at least one other gate electrode is formed from a conductive material different from the metal carbide and different from the metal from which the carbide was formed.

It should be noted that forming a metal carbide gate by the solid state reaction of a first metal with a carbon-containing layer has a number of advantages over processes in which the metal carbide layer is formed in one step. Sputter deposition processes can deposit high quality metal carbides, but are likely to damage the exposed gate dielectric (due to the energetic charged particle bombardment). CVD processes are damage-free, but cannot easily co-deposit a metal with carbon without incorporating substantial amounts of impurities such as oxygen. With the present bi-layer reaction process, a bottom metal layer may be cleanly deposited by CVD, with subsequent deposition of a carbon-containing layer by any preferred method (including sputtering, since the presence of the previously deposited metal layer protects the gate dielectric).

The foregoing description of the invention illustrates and describes the present invention. Additionally, the disclosure shows and describes only the preferred embodiments of the invention but, as mentioned above, it is to be understood that the invention is capable of use in various other combinations, modifications, and environments and is capable of changes or modifications within the scope of the invention concept as expressed herein, commensurate with the above teachings and/or skill or knowledge of the relevant art. The embodiments described hereinabove are further intended to explain best modes known of practicing the invention and to enable others skilled in the art to utilize the invention in such, or other, embodiments and with the various modifications required by the particular applications or uses of the invention. Accordingly, the description is not intended to limit the invention to the form disclosed herein. Also, it is intended that the appended claims be construed to include alternative embodiments.